WHAT IS CLAIMED IS:

1. A memory buffer for receiving a frame comprised of sequential input symbols and providing the input symbols to an N-window mode Soft-In Soft-Out (SISO) decoder having a window size of W symbols, comprising:

a first shift register having an input terminal, an output terminal and a clock input terminal, for sequentially shifting and storing 2NW serial symbols from the input terminal in a predetermined direction, and sequentially outputting the shifted symbols via the output terminal; and

N second shift registers, wherein each of the second shift registers includes a clock input terminal, first and second input terminals, first and second output terminals, and select terminals, the second shift registers are sequentially activated or initialized at intervals of W symbols from serial symbols received at the input terminal of the first shift register, each of the second shift registers receives first NW symbols among the serial symbols after its activation, and shifts and stores the received symbols in a predetermined direction, thereafter, each of the second shift registers receives second NW symbols via its second input terminal, shifts and stores the received symbols in the opposite direction of the predetermined direction, and at the same time, serially outputs the stored first NW symbols via its first output terminal, thereafter, each of the second shift registers receives third NW symbols via the first input terminal, shifts and stores the received symbols in the predetermined direction, and at the same time, serially outputs the stored second NW symbols via its first output terminal.

2. The memory buffer of claim 1, wherein the W symbols include first to W^{th} consecutive symbols of the received frame.

3. The memory buffer of claim 1, wherein each of the shift registers operates in response to transitions of a clock.

4. The memory buffer of claim 1, wherein N is 2.

5. The memory buffer of claim 1, wherein the W window symbols are determined by dividing a received frame into a predetermined number of frames.

6. A turbo decoding apparatus in a communication system, comprising:

a unidirectional shift register having an input terminal for data input and an output terminal for data output, the unidirectional shift register forming bit streams of a first length by sequentially receiving and shifting input data bits via the input terminal and then sequentially outputting the formed bit streams of the first length via the output terminal;

a memory buffer including one or more bidirectional shift registers having a first terminal and a second terminal for data input/output, the input data bits being divided into groups each comprised of bits of a second length which is 1/2 of the first length, the bidirectional shift register forming bit streams of the second length by sequentially receiving and shifting bits of odd-numbered groups among the divided groups via the first terminal and then sequentially outputting the formed bit streams via the first terminal; and forming bit streams of the second length by sequentially receiving and shifting bits of even-numbered groups among the divided groups via the second terminal and then sequentially outputting the formed bit streams via the second terminal;

a first metric calculation section for receiving output bits of the respective shift registers, and calculating corresponding delta metrics;

a second metric calculation section for receiving a delta metric from the first metric calculation section corresponding to the unidirectional shift register, and calculating an alpha metric;

a third metric calculation section for receiving delta metrics from the first metric calculation section corresponding to the bidirectional shift registers, and

calculating beta metrics;

a fourth metric calculation section for receiving the alpha metric, also receiving a multiplexing result of the beta metrics, and calculating Log Likelihood Ratio (LLR) values corresponding to the respective shift registers; and

a Soft-In Soft-Out (SISO) decoder including a subtraction section for subtracting an output of the unidirectional shift register from the respective LLR values, and outputting the subtraction result for interleaving/deinterleaving.

7. The turbo decoding apparatus of claim 6, wherein the memory buffer further comprises a control logic for determining whether the input data bits are bits of odd-numbered groups or bits of even-numbered groups among the divided groups, and providing the bidirectional shift registers with select signals for applying the input data bits to the first terminal or the second terminal according to the determination result.

8. The turbo decoding apparatus of claim 7, wherein the memory buffer further comprises a demultiplexer and a multiplexer corresponding to each of the bidirectional shift registers;

wherein the demultiplexer has an input terminal for receiving the input data bits and a first output terminal and a second output terminal connected to the first terminal and the second terminal, respectively, applies bits of the odd-numbered groups to the first terminal via the first output terminal in response to a corresponding select signal provided from the control logic, and applies bits of the even-numbered groups to the second terminal via the second output terminal;

wherein the multiplexer multiplexes bit streams output via the first terminal and bit streams output via the second terminal in response to a corresponding select signal provided from the control logic, and outputs the multiplexed bit streams to the first metric calculation section.

9. The turbo decoding apparatus of claim 7, wherein the select signals are control signals for applying the input data bits to the bidirectional shift registers at different times.

10. The turbo decoding apparatus of claim 6, wherein the bits of the odd-numbered groups are sequentially output via the first terminal and, at the same time, the bits of the even-numbered groups are sequentially received and shifted via the second terminal.

11. The turbo decoding apparatus of claim 6, wherein the number of the bidirectional shift registers is determined by the number of widows.

12. The turbo decoding apparatus of claim 6, wherein the first length and the second length are determined by a size of windows and the number of windows.

13. The turbo decoding apparatus of claim 12, wherein the second length is determined by multiplying the size of windows by the number of windows.

14. The turbo decoding apparatus of claim 6, wherein the input data bits are received at a clock rate of a turbo decoder.

15. A turbo decoding apparatus in a communication system, comprising:

one or more first stage's bidirectional shift registers having a first terminal and a second terminal for data input/output, input data bits being divided into groups each comprised of bits of a predetermined length, the first stage's bidirectional shift registers forming bit streams of the length by sequentially receiving and shifting bits of odd-numbered groups among the divided groups via

the first terminal and then sequentially outputting the formed bit streams via the first terminal; and forming bit streams of the length by sequentially receiving and shifting bits of even-numbered groups among the divided groups via the second terminal and then sequentially outputting the formed bit streams via the second terminal;

a memory buffer including a second stage's bidirectional shift register having a third terminal and a fourth terminal for data input/output, the second stage's bidirectional shift register forming bit streams of the length by sequentially receiving and shifting bits sequentially output via the first terminal, via the third terminal, and then sequentially outputting the formed bit streams via the third terminal; and forming bit streams of the length by sequentially receiving and shifting bits sequentially output via the second terminal, via the fourth terminal, and then sequentially outputting the formed bit streams via the fourth terminal;

a first metric calculation section for receiving output bits of the respective shift registers, and calculating corresponding delta metrics;

a second metric calculation section for receiving a delta metric from the first metric calculation section corresponding to the unidirectional shift register, and calculating an alpha metric;

a third metric calculation section for receiving delta metrics from the first metric calculation section corresponding to the bidirectional shift registers, and calculating beta metrics;

a fourth metric calculation section for receiving the alpha metric, also receiving a multiplexing result of the beta metrics, and calculating Log Likelihood Ratio (LLR) values corresponding to the respective shift registers; and

a Soft-In Soft-Out (SISO) decoder including a subtraction section for subtracting an output of the unidirectional shift register from the respective LLR values, and outputting the subtraction result for interleaving/deinterleaving.

16. The turbo decoding apparatus of claim 15, wherein the memory buffer further comprises a control logic for determining whether the input data bits are bits of odd-numbered groups or bits of even-numbered groups among the divided groups, and providing the first stage's bidirectional shift registers with select signals for applying the input data bits to the first terminal or the second terminal according to the determination result.

17. The turbo decoding apparatus of claim 16, wherein the memory buffer further comprises a demultiplexer and a multiplexer corresponding to each of the first stage's bidirectional shift registers;

wherein the demultiplexer has an input terminal for receiving the input data bits and a first output terminal and a second output terminal connected to the first terminal and the second terminal, respectively, applies bits of the odd-numbered groups to the first terminal via the first output terminal in response to a corresponding select signal provided from the control logic, and applies bits of the even-numbered groups to the second terminal via the second output terminal;

wherein the multiplexer multiplexes bits output via the first terminal and bits output via the second terminal in response to a corresponding select signal provided from the control logic, and outputs the multiplexed bits to the first metric calculation section.

18. The turbo decoding apparatus of claim 16, wherein the memory buffer further comprises a multiplexer corresponding to the second stage's bidirectional shift register, the multiplexer multiplexing bits output via the third terminal and bits output via the fourth terminal in response to a corresponding select signal provided from the control logic, and outputting the multiplexed bits to the first metric calculation section.

19. The turbo decoding apparatus of claim 16, wherein the select signals are control signals for applying the input data bits to the bidirectional

shift registers at different times.

20. The turbo decoding apparatus of claim 15, wherein the bits of the odd-numbered groups are sequentially output via the first terminal and, at the same time, the bits of the even-numbered groups are sequentially received and shifted via the second terminal.

21. The turbo decoding apparatus of claim 15, wherein the number of the first stage's shift registers is determined by the number of windows.

22. The turbo decoding apparatus of claim 15, wherein the input data bits are received at a clock rate of a turbo decoder.

23. A method of providing a memory buffer for receiving a frame comprised of sequential input symbols and providing the input symbols to an N-window mode Soft-In Soft-Out (SISO) decoder having a window size of W symbols, the method comprising the steps of:

sequentially shifting and storing 2NW serial symbols from an input terminal of a first shift register in a predetermined direction;

sequentially outputting the shifted symbols via the output terminal of the first shift register; and

sequentially activating or initializing N second shift registers at intervals of W symbols from serial symbols received at the input terminal of the first shift register, wherein each of the second shift registers includes a clock input terminal, first and second input terminals, first and second output terminals, and select terminals

receiving at each of the second shift registers first NW symbols among the serial symbols after its activation;

shifting and storing the received symbols in a predetermined direction,

thereafter, each of the second shift registers receiving second NW symbols via its second input terminal; and

shifting and storing the received symbols in the opposite direction of the predetermined direction, and simultaneously, serially outputting the stored first NW symbols via its first output terminal, thereafter, each of the second shift registers receiving third NW symbols via the first input terminal, shifting and storing the received symbols in the predetermined direction, and simultaneously, serially outputting the stored second NW symbols via its first output terminal.

24. The method of claim 23, wherein N comprises 2.

25. The method of claim 23, further comprising:

dividing a received frame into a predetermined number of frames to determine the W window symbols.

26. A method of providing a turbo decoding in a communication system, the method comprising:

forming at a unidirectional shift register having an input terminal for data input and an output terminal for data output, bit streams of a first length by sequentially receiving and shifting input data bits via the input terminal and then sequentially outputting the formed bit streams of the first length via the output terminal;

dividing input data into groups the input data each comprised of bits of a second length which is 1/2 of the first length, at a memory buffer including one or more bidirectional shift registers having a first terminal and a second terminal for data input/output, the bidirectional shift register forming bit streams of the second length by sequentially receiving and shifting bits of odd-numbered groups among the divided groups via the first terminal and then sequentially outputting the formed bit streams via the first terminal; and forming bit streams of the second length by sequentially receiving and shifting bits of even-numbered

groups among the divided groups via the second terminal and then sequentially outputting the formed bit streams via the second terminal;

receiving output bits of the respective shift registers, and calculating corresponding delta metrics at a first metric calculation section;

receiving a delta metric from the first metric calculation section corresponding to the unidirectional shift register, and calculating an alpha metric a second metric calculation section;

receiving delta metrics from the first metric calculation section corresponding to the bidirectional shift registers, and calculating beta metrics a third metric calculation section;

receiving the alpha metric, also receiving a multiplexing result of the beta metrics, and calculating Log Likelihood Ratio (LLR) values corresponding to the respective shift registers at a fourth metric calculation section; and

subtracting an output of the unidirectional shift register from the respective LLR values, and outputting the subtraction result for interleaving/deinterleaving at a Soft-In Soft-Out (SISO) decoder including a subtraction section.

27. The method of claim 26 further comprising:

determining whether the input data bits are bits of odd-numbered groups or bits of even-numbered groups among the divided groups the memory buffer for a control logic; and

providing the bidirectional shift registers with select signals for applying the input data bits to the first terminal or the second terminal according to the determination result.

28. The method of claim 26, wherein the memory buffer further comprises a demultiplexer and a multiplexer corresponding to each of the bidirectional shift registers;

wherein the demultiplexer has an input terminal for receiving the input

data bits and a first output terminal and a second output terminal connected to the first terminal and the second terminal, respectively, applies bits of the odd-numbered groups to the first terminal via the first output terminal in response to a corresponding select signal provided from the control logic, and applies bits of the even-numbered groups to the second terminal via the second output terminal;

wherein the multiplexer multiplexes bit streams output via the first terminal and bit streams output via the second terminal in response to a corresponding select signal provided from the control logic, and outputs the multiplexed bit streams to the first metric calculation section.

29. The method of claim 26, wherein the select signals are control signals for applying the input data bits to the bidirectional shift registers at different times.

30. The method of claim 26, wherein the bits of the odd-numbered groups are sequentially output via the first terminal and, at the same time, the bits of the even-numbered groups are sequentially received and shifted via the second terminal.

31. The method of claim 26, wherein the number of the bidirectional shift registers is determined by the number of widows.

32. The method of claim 26, wherein the first length and the second length are determined by a size of windows and the number of windows.

33. The method of claim 32, wherein the second length is determined by multiplying the size of windows by the number of windows.

34. The method of claim 26, wherein the input data bits are received at a clock rate of a turbo decoder.

35. A method of providing turbo decoding in a communication system, comprising:

dividing input data bits into groups each comprised of bits of a predetermined length, via one or more first stage's bidirectional shift registers having a first terminal and a second terminal for data input/output, the first stage's bidirectional shift registers forming bit streams of the length by sequentially receiving and shifting bits of odd-numbered groups among the divided groups via the first terminal and then sequentially outputting the formed bit streams via the first terminal; and forming bit streams of the length by sequentially receiving and shifting bits of even-numbered groups among the divided groups via the second terminal and then sequentially outputting the formed bit streams via the second terminal;

forming at a second stage's bidirectional shift register having a third terminal and a fourth terminal for data input/output, bit streams of the length by sequentially receiving and shifting bits sequentially output via the first terminal, via the third terminal, and then sequentially outputting the formed bit streams via the third terminal; and forming bit streams of the length by sequentially receiving and shifting bits sequentially output via the second terminal, via the fourth terminal, and then sequentially outputting the formed bit streams via the fourth terminal;

receiving output bits of the respective shift registers, and calculating corresponding delta metrics at a first metric calculation section;

receiving a delta metric from the first metric calculation section corresponding to the unidirectional shift register, and calculating an alpha metric at a second metric calculation section;

receiving delta metrics from the first metric calculation section corresponding to the bidirectional shift registers, and calculating beta metrics at a third metric calculation section;

receiving the alpha metric, also receiving a multiplexing result of the

beta metrics, and calculating Log Likelihood Ratio (LLR) values corresponding to the respective shift registers at a fourth metric calculation section; and

subtracting an output of the unidirectional shift register from the respective LLR values, and outputting the subtraction result for interleaving/deinterleaving at a Soft-In Soft-Out (SISO) decoder including a subtraction section.

36. The method of claim 35, further comprising:

determining whether the input data bits are bits of odd-numbered groups or bits of even-numbered groups among the divided groups for a control logic; and

providing the first stage's bidirectional shift registers with select signals for applying the input data bits to the first terminal or the second terminal according to the determination result.

37. The method of claim 36, wherein the memory buffer further comprises a demultiplexer and a multiplexer corresponding to each of the first stage's bidirectional shift registers;

wherein the demultiplexer has an input terminal for receiving the input data bits and a first output terminal and a second output terminal connected to the first terminal and the second terminal, respectively, applies bits of the odd-numbered groups to the first terminal via the first output terminal in response to a corresponding select signal provided from the control logic, and applies bits of the even-numbered groups to the second terminal via the second output terminal;

wherein the multiplexer multiplexes bits output via the first terminal and bits output via the second terminal in response to a corresponding select signal provided from the control logic, and outputs the multiplexed bits to the first metric calculation section.

38. The method of claim 36, further comprising:

multiplexing bits output via the third terminal and bits output via the fourth terminal in response to a corresponding select signal provided from the control logic via a multiplexer of the memory buffer corresponding to the second stage's bidirectional shift register; and

outputting the multiplexed bits to the first metric calculation section.

39. The method of claim 36, wherein the select signals comprises control signals for applying the input data bits to the bidirectional shift registers at different times.

40. The method of claim 35, wherein the bits of the odd-numbered groups are sequentially output via the first terminal and, at the same time, the bits of the even-numbered groups are sequentially received and shifted via the second terminal.

41. The method of claim 35 further comprising:

determining the number of the first stage's shift registers by the number of windows.

42. The method of claim 35, further comprising:

receiving the input data bits at a clock rate of a turbo decoder.